

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number
WO 02/14952 A2

- (51) International Patent Classification⁷: **G03F 7/00**
- (21) International Application Number: PCT/US01/25496
- (22) International Filing Date: 14 August 2001 (14.08.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
09/639,381 14 August 2000 (14.08.2000) US
- (71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
P.O. Box 450A, Santa Clara, CA 95052 (US).
- (72) Inventors: **RISHTON, Stephen, A.**; 2511 Bishop Avenue, Fremont, CA 94536 (US). **LOZES, Richard, L.**; P.O. Box 5340, Pleasanton, CA 94566-1340 (US).
- (74) Agents: **BERNADICOU, Michael, A.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AT (utility model), AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:**
— without international search report and to be republished upon receipt of that report
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: SCAN BUTTING ERROR REDUCTION IN A RASTER SCAN PATTERN GENERATION SYSTEM

(57) Abstract: A method and apparatus are disclosed for reducing scan butting error in a raster scan pattern generation system. A pattern to be written on a mask is first pixelized and each pixel is assigned a gray level value describing how much of the pixel is occupied by a feature to be written on the mask. The ends of each scan are overlapped with the neighboring scans. In each scan, no pattern data is written to the mask in the lower overlap region of the scan until a blank pixel or a pair of blank pixels is detected, i.e. a pixel or pair of pixels that do not contain any part of a feature to be written on the mask. After such a pixel or pair of pixels is detected, the pattern data for each flash is written to the mask until another blank pixel or pair of blank pixels is detected in the upper overlap region of the scan. No pattern data is written to the mask for the flashes in the scan that are scanned after the pair of blank pixels.

SCAN BUTTING ERROR REDUCTION IN A RASTER SCAN PATTERN GENERATION
SYSTEM

5

Stephen A. Rishton
Richard L. LozesBACKGROUND

When producing integrated circuits, typically a photomask is used to form patterns on the
10 surface of silicon wafers. The photomask, which is also referred to as a mask or reticle,
conventionally consists of a clear or transparent substrate such as borosilicate or quartz, with a
thin opaque layer about 100 nm in thickness of chrome and chrome oxides sputter-coated on one
side of the mask called the active side. The photomask is produced by covering the chrome oxide
coating or film with a resist film. The desired pattern is formed by exposing a series of lines, or
15 trapezoids, on such resist coated substrate, with some form of radiation. The radiation breaks the
molecular bonds on the resist coating where it contacts and increases the dissolution rate of the
resist thus exposed, when the resist is subsequently immersed in a suitable developer solution.
The patterned areas thus formed in the resist, by exposure to the radiation, are removed and the
chrome film is etched with an acid. After etching the remaining resist is then removed.

20 The pattern areas in the resist are formed by scanning of an optical or electron beam
across the active mask face. With an electron beam raster scan pattern generator, a beam of
electrons is scanned in one direction, termed the "Y direction," while the substrate is moved
across the electron beam perpendicular to the first direction, termed the "X direction." The
complete pattern is formed by a combination of the small electron beam displacement and the
25 much larger stage motion of the substrate. The complete pattern has a series of X-directed stripes
with the Y-directed electron beam scan.

The pattern data itself is made up of small segments called pixels. The features cover
several pixels collectively. These pattern features are written on the mask by turning the writing

beam on for the required number of pixels. The electron beam scans a fixed number of pixels in the Y direction and then retraces to the beginning of the next scan. The stage is then moved the required amount of X displacement and the next scan begins.

Errors often occur at the boundaries of stripes in the X direction and scans in the Y direction. Such butting errors can result in features near scan and stripe boundaries that are larger or smaller than the coded feature. Typically, the stage cannot be positioned so accurately that corresponding scans in two adjoining stripes match perfectly. Thus, features that straddle two scans in the Y direction are problematic. The alignment of the stage is not accurate enough to allow the straddling feature to be exposed in two separate scans.

Methods have been proposed to reduce or eliminate such butting errors. An example of such a method is presented in U.S. Patent No. 5,766,802, "Photomask" to Skinner. Skinner states "writing errors in producing printed circuits are substantially reduced by moving the writing scan boundary around a critical feature and thereby eliminating features which extend over scan boundary areas" See Skinner, col. 3, lines 39-43. Skinner further states "[t]he changing of the writing width is accomplished by software which eliminates pattern data in the overlap region of the lower portion of each stripe except where a critical feature is located. This can also be done mechanically such as by adjusting the shutter on the beam generating device and then closing the shutter after the desired feature has been scanned. This, in effect, moves the small features into the next adjacent scan area." See Skinner, col. 4, lines 28-36. Skinner's method overlaps adjacent stripes, then deletes pattern data in the overlap region from one strip or another such that features appear in only one stripe. This method requires additional data processing steps to move the features in the overlap area to one stripe or another.

SUMMARY

A method and apparatus are disclosed for reducing scan butting error in a raster scan pattern generation system. A pattern to be written on a mask is first pixelized and each pixel is assigned a gray level value describing how much of the pixel is occupied by a feature to be written on the mask. The pattern is then divided into overlapping stripes of flashes. Each flash includes one or several pixels. In each scan, no pattern data is written to the mask in the lower overlapping region of the scan until a flash is detected with a blank pixel or pixels in the flash or in the pixels immediately above the flash. A blank pixel is a pixel that does not contain any part of a feature to be written on the mask. The pattern data of the flash with the blank pixel or pixels in the flash or directly above the flash is ignored, then the system begins writing the actual pattern data for each flash to the mask, beginning with the next flash. In the upper overlapping portion of the scan, the pattern data for each flash is written to the mask until a flash is detected with a blank pixel or pixels in the flash or in the pixels immediately above the flash. The pattern data for the flash with the blank pixel or pixels in the flash or above the flash is written to the mask. The pattern data in the remaining flashes in the upper overlap region are ignored, beginning with the flash after the flash with the blank pixel or pixels in the flash or in the pixels immediately above the flash.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates, in a block diagram, a lithography system.

FIG. 2A illustrates, in a flowchart, a process performed by the flash converter of FIG. 1 according to one embodiment of the invention.

FIGS. 2B, 2C, and 2D illustrate, in flowcharts, the process of FIG. 2A in more detail.

FIG. 3 illustrates a photomask formed according to the process of FIG. 2A.

DETAILED DESCRIPTION

FIG. 1 depicts a block diagram of a lithography system 100 suitable for implementing the present invention. Lithography system 100 is described in more detail in U.S. Patent Application Serial No. 09/226,926, filed January 6, 1999, entitled "A METHOD AND APPARATUS THAT DETERMINES CHARGED PARTICLE BEAM SHAPE CODES," assigned to Etec Systems, Inc., and incorporated herein in its entirety by this reference. The lithography system includes a rasterizer circuit 102, a buffer circuit 104, a dose value circuit 106, a flash converter 108, a shaper/blanker driver 110, and electron beam column 112. Flash converter 108 and shaper/blanker driver 110 are each coupled to receive a clock (timing) signal from clock 114.

Rasterizer circuit 102 first receives (e.g. from a conventional lithography data structure) a pattern that is to be written onto a substrate 118 specified by its shape location on the substrate (so called "vector format"). Rasterizer 102 then divides the surface of the substrate 118 into a grid of pixels and represents each pixel as a "gray level value" which specifies a fraction of the pixel's area which includes part of the pattern. Rasterizer 102 outputs each gray level value to both buffer 104 and dose value circuitry 106. (The connecting lines in FIG. 1 inside the dotted lines typically represent multi-line data busses.) Buffer 104 provides gray level values to flash converter 108. In one embodiment, flash converter 108 represents each square arrangement (2 dimensional) of four pixels ("quadrant") as a flash field that may be exposed in one flash cycle (hereafter the term "flash field" represents a blank or a shape that electron beam column 112 writes onto substrate 118). In other embodiments, a flash field may contain only a single pixel or a flash field may contain multiple pixels. For simplicity, a flash field is also referred to as a flash. Flash converter 108 specifies each flash field by shape class and coordinates (shape_x, shape_y) (hereafter the term "shape data" refers to both shape class and coordinates). Each shape class has a shape code, typically a number, which specifies the shape and the orientation of the portion of the flash to be written on the mask. Dose value circuitry 106 receives gray level

values associated with each quadrant from the rasterizer circuit 102 and outputs dose values associated with each flash field.

Shaper/blanker driver 110 requests shape data and corresponding dose values (hereafter shape data and corresponding dose values are referred together as a "flash data") from respective flash converter 108 and dose value circuitry 106. In one embodiment, flash converter 108 and dose value circuitry 106 provide a flash data to shaper/blanker driver 110 approximately every 10 ns. Shaper/blanker driver 110 converts each flash data to voltage values and provides the voltages to control electron beam column 112 to write the specified flash field in a proper location on the substrate 118. In this embodiment, electron beam column 112 writes a new flash field every 10 ns (hereafter "flash cycle"). For a blank flash, electron beam column 112 does not write the electron beam onto substrate 118. An ion beam column or other energy beam (e.g., laser) may be substituted for column 112.

Rasterizer 102 divides a pattern into a grid of pixels and represents each pixel as a "gray level value" which specifies a fraction of the pixel's area which includes part of the pattern. In one embodiment, the gray level value may range from 0 to 16. A gray level value of 0 indicates that the pixel is blank, i.e. that the pixel includes no portion of a feature and thus none of the pixel is exposed. A gray level value of 16 indicates that the entire pixel is included in a feature and thus the entire pixel is exposed. The number corresponding to a gray level value is assigned arbitrarily.

The grid representing the pattern is divided into horizontal stripes, which are further divided into vertical scans. In one embodiment, a stripe is 8192 pixels high. In one embodiment, each vertical scan is a series of flashes of four pixels arranged in a square, i.e. two pixels wide by two pixels high. In another embodiment, each vertical scan is a series of flashes of a single pixel. The stripes overlap. In one embodiment, the overlap region is 320 pixels high.

Thus, the top and bottom 320 pixels of each stripe overlap with the stripe above and the stripe below.

FIGS. 2A-2D illustrate the process performed by flash converter 108 of FIG. 1 in more detail. Flash converter 108 receives gray level values from buffer 104 for one flash of pixels at a time, then converts the gray level values to a single shape code for each flash, then sends the shape data to shaper/blanker driver 110. In FIG. 2A, for each scan in a stripe, flash converter 108 first converts the gray level values of flashes in the lower overlap region of the scan in stage 12, then converts the gray level values of flashes in the center of the scan in stage 14, then converts the gray level values of flashes in the upper overlap region of the scan in stage 16. An example of a flash converter and the conversion of gray level values to shape data are described in more detail in "A METHOD AND APPARATUS THAT DETERMINES CHARGED PARTICLE BEAM SHAPE CODES." Flash converter 108 may be hardwired logic that performs process 10 or flash converter 108 may be a computer executing a software form of process 10.

In an embodiment where each flash is four pixels arranged in a square, in the lower overlap region, no pixels are written until flash converter 108 detects a horizontal pair of zero gray level value pixels. After such a pair is detected, the flashes are written normally. In the upper overlap region, flashes are written until flash converter 108 detects a horizontal pair of zero gray level value pixels. After such a pair of pixels is detected, no more flashes are written in the upper overlap region of the scan. Thus, in an overlap region between two stripes, all features below the first horizontal pair of zero gray level value pixels are written in the upper overlap portion of scans in the lower stripe, and all features above the first pair of horizontal zero gray level value pixels are written in the lower overlap portion of scans in the upper stripe. In an embodiment where each flash is a single pixel, a flash with pixel of zero gray level value starts writing in the lower overlap region and a flash with a pixel of zero gray level value ends writing

in the upper overlap region. FIGS. 2B and 2D illustrate an embodiment where each flash is four pixels arranged in a square.

FIG. 2B illustrates stage 12 of FIG. 2A, the conversion of gray level values to shape data for flashes in the lower overlap region of a scan, in more detail. In stage 20, flash converter 108 receives from buffer 104 gray level values for each pixel of a flash of a scan. Flash converter 108 also receives gray level values for the pixels surrounding the flash. The surrounding gray level values are used to determine the shape exposed on the mask for the flash. For flashes in the overlap region, flash converter 108 also decides to write the flash or not based on the gray level values of the flash and the gray level values in the pixels above the flash. Flash converter 108 checks in stage 22 if the flash or the two pixels above the flash contain a horizontal pair of pixels, each with a gray level value of zero. If the flash or the two pixels above the flash do not include a horizontal pair of zero gray-value pixels, a shape code for a blank flash is sent to shaper/blanker driver 110 in stage 23. Thus, if there is not a pair of zero-value pixels in the flash or in the pixels above the flash, the pattern contained in the flash is ignored and nothing is written to the mask for the flash, even if the flash contains a part of a feature. The process then returns to stage 20 and the next set of gray level values are received by flash converter 108. All flashes are treated as blank flashes until flash converter 108 receives a flash with a pair of zero-value pixels in the flash or in the two pixels above the flash.

If there is a horizontal pair of zero gray level value pixels in the flash or in the two pixels above the flash, the current flash is treated as a blank flash in stage 24. After flash converter 108 receives a flash with a horizontal pair of zeros in the flash or in the two pixels above the flash, all flashes after that flash are treated normally according to FIG. 2C, i.e. the proper shape code for the flash is sent to shaper/blanker driver 110, and the pattern represented by the flash is written to the mask. Thus, when a flash is identified with a horizontal pair of zeroes in the flash or in the two pixels above the flash, the data in that flash are ignored and no shape data are written to the

mask for that flash, then all the remaining flashes in the lower overlap region are written normally, beginning with the next flash. If no flashes with a horizontal pair of zeros in the lower half of the flash are detected in the lower overlap region of the scan, all the data in the lower overlap region of the scan are ignored. The scanner writes data beginning with the first flash
5 above the lower overlap region.

The first flash in the lower overlap region must be handled differently from the other flashes in the lower overlap region. The flashes must be handled such that the upper overlap region of a scan and the lower overlap region of the scan above are consistent, i.e. so all flashes are exposed either the upper overlap region of the lower scan, or in the lower overlap region of
10 the upper scan, not both. The handling of the first flash in the lower overlap region is illustrated by FIG. 3. FIG. 3 illustrates an example of a photomask formed according to an embodiment of the present invention. Portions of two stripes are shown, lower stripe 81 and upper stripe 82. Stripes 81 and 82 overlap in region 80. Each stripe is divided into vertical scans, scans 61-71. Of course, FIG. 3 is merely illustrative, as FIG. 3 shows an overlap region that is only two
15 flashes wide, while a typical overlap region may be 320 flashes wide. For simplicity, each flash in FIG. 3 is referred to by its row number and column number, thus the flash in row 44 and column 61 is referred to as flash 44,61. The first flashes in the lower overlap region of stripe 82 are in row 44.

There are four possible cases for the first flash in the lower overlap region, illustrated by
20 FIG. 3: first, the first flash has four pixels with nonzero gray level values, illustrated by pixel 44,67; second, the first flash has four pixels with zero gray level values, illustrated by pixel 44,65; third, the first flash has a horizontal pair of zero gray level value pixels in the lower half of the flash and nonzero pixels in the upper half of the flash, illustrated by pixel 44,61; and fourth, the first flash has a horizontal pair of zero gray level value pixels in the upper half of the

flash and nonzero pixels in the lower half of the flash, illustrated by pixel 44,64. Only the third case must be handled differently from the process described in FIG. 2B.

Dotted line 83 illustrates the first horizontal pair of zero gray level value pixels encountered in the overlap region for each scan. No features in the overlap region below the first horizontal pair of zeroes in each scan should be written in upper stripe 82. Thus, features 91 and 92 should be written in scans in upper stripe 82, while features 93 and 94 should be written in scans in lower stripe 81. As a result, flash 44,61, illustrating the third case, should be written in upper stripe 82. However, according to the process described in FIG. 2B, flash 44,61 would not be written in the lower overlap region of upper stripe 82 because flash converter 108 would detect a horizontal pair of zeroes in the flash in stage 22, then send blank shape code data to shaper/blanker driver 110 in stage 24. If flash 44,61 contained the first horizontal pair of zero gray level values and was located above the first pixel in the lower overlap region, flash 44,61 would be written because according to the process described in FIG. 2B, when the flash before flash 44,61 was received in stage 20 and checked for a pair of horizontal zeroes, flash converter 108 would detect the horizontal pair of zeroes just above that flash, i.e. the horizontal pair of zero pixels in the lower half of flash 44,61. Thus, in stage 24, flash converter 108 would provide blank flash data for the flash below flash 44,61, then write all remaining flashes in the lower overlap region normally in stage 26 of FIG. 2B, beginning with flash 44,61.

There are several ways to avoid mishandling a first flash in the lower overlap region such as flash 44,61. In one embodiment, for the first flash in the lower overlap region only, flash converter 108 checks for a horizontal pair of zeroes in the lower half of the first flash. If there is a horizontal pair of zeroes in the lower half of the flash, flash converter 108 writes all the flashes in the lower overlap region normally according to the process described in FIG. 2C. If there is not a horizontal pair of zeroes in the lower half of the flash, flash converter 108 treats the flash according to the process described in FIG. 2B. In other embodiments, flash converter 108

receives the gray level values for the flash below the first flash in the lower overlap region, ignores data contained in the flash below the first flash, and begins writing with the first flash in the lower overlap region if flash converter 108 detects a horizontal pair of zeroes in the pixels just above the flash below the first flash in the lower overlap region.

5 FIG. 2C illustrates stage 14 of FIG. 2A, the conversion of gray level values to shape data for flashes in the center of a scan, in more detail. The center of the scan refers to all the flashes in the scan that come after the first flash in the lower overlap region with a pair of zero-value pixels in the lower half of the flash, as well as all the flashes in the scan do not fall in the upper or lower overlap regions of the scan. In stage 17, flash converter 108 receives a set of gray level
10 values for the pixels in each flash. In stage 18, the gray level values are represented as shape data for the flash. In stage 19, the shape code data are provided to shaper/blanker driver 110.

 FIG. 2D illustrates stage 16 of FIG. 2A, the conversion of gray level values to shape data for flashes in the upper overlap region of a scan, in more detail. In stage 31, flash converter 108 receives the gray level values of the pixels of a flash in the upper overlap region. In stage 32,
15 flash converter 108 checks if there is a horizontal pair of pixels each with a gray level value of zero in the flash or in the pixels immediately above the flash. If there is no horizontal pair of pixels each with a gray level value of zero in the flash or in the pixels immediately above the flash, the pattern in the flash is represented as a shape code in stage 34. In stage 35, the shape code data are provided to shaper/blanker driver 110, then the process returns to stage 31, where
20 flash converter 108 receives the next gray level values for the pixels in the next flash in the upper overlap region.

 If there is a horizontal pair of pixels each with a gray level value of zero in the flash or in the pixels immediately above the flash, flash converter 108 provides shape data for the current flash to shaper/blanker driver 110 in stage 33, then provides blank flash shape data to
25 shaper/blanker driver for each of the remaining flashes in the upper overlap region in stage 36.

Thus, once a flash with a pair of zero gray level value pixels in the flash or in the pixels above the flash, the pattern data for that flash is written to the mask, then the pattern in all the remaining flashes in the upper overlap region is ignored and blank shape data for each remaining flash is sent to shaper/blanker driver 110. In one embodiment, the scanner scans all the
5 remaining flashes in the upper overlap region and provides blank shape data to shaper/blanker driver 110 for all remaining flashes. In another embodiment, upon detecting a flash with a pair of zero gray level value pixels, the scanner simply ignores all the remaining flashes in the upper overlap region and returns to the bottom of the scan to begin the next scan.

Similar to the lower overlap region, the first flash in the upper overlap region must be
10 treated differently. In one embodiment, flash converter 108 checks the first flash in the upper overlap region for a horizontal pair of zeros in the lower half of the flash. If the first flash has a horizontal pair of zeros in the lower half of the flash, blank flashes are written to the mask for all flashes in the upper overlap region of the scan. If the one of the pixels in the lower half of the first flash is nonzero, the flash is treated according to the process described in FIG. 2C. In
15 another embodiment, when writing the last flash before the upper overlap region, flash converter 108 looks for a pair of zero gray level pixels immediately above the last flash before the upper overlap region. If there is such a pair above the last flash before the upper overlap region, blank data is written to the mask for all the flashes in the upper overlap region.

In an embodiment where each flash contains only a single pixel, in the lower overlap
20 region, no data are written for each flash until a flash with a zero gray level value is detected. The data in the flashes in the lower overlap region after the zero gray level value pixel and the data in all the flashes in the nonoverlapping region are then written normally according to the process described in FIG. 2C. In the upper overlap region, the data in the flashes are written normally until a flash is detected with a zero gray level value. The data in all the flashes in the
25 upper overlap region after the zero gray level value are ignored.

FIG. 3 illustrates a mask formed by the processes described in FIGS. 2B-2D. Overlap region 80 forms the upper overlap region of stripe 81 and the lower overlap region of stripe 82. For the scans in lower stripe 81, the flashes in rows 41-43 of the scans in stripe 81 are not in the overlap region and are therefore converted from pixel gray level values to shape data in stripe 81 according to the process described in FIG. 2C. The flashes in overlap region 80 in each scan of lower stripe 81 are converted according to process 16 described in FIG. 2D and the rules for handling the first flash in the overlap region. Thus, for the first scan 61, flash 44,61 is the first flash in overlap region 80. The lower pixels of flash 44,61 both have a gray level value of zero and the upper pixels of flash 44,61 each have a nonzero gray level value, therefore flash 44,61 represents the third case for a first flash in the overlap region and must be handled differently from the process described in FIG. 2D. The data in flash 44,61 and all the flashes above it in the overlap region are ignored in scan 61 of stripe 81.

The substrate is then repositioned for the next scan, scan 62. After writing the flashes in the non-overlapping region to the mask, the scan reaches the first flash in the overlap region, flash 44,62. Flash 44,62 is the first flash in scan 62 in the upper overlap region, thus flash 44,62 is checked for a horizontal pair of zeros in the lower half of the flash and nonzero pixels in the upper half of the flash. Since flash 44,62 has a horizontal pair of zeros in the lower half of the flash, the data in flash 44,64 and every other flash in the upper overlap region of scan 62 are ignored and blank pattern data are written to the mask for those flashes. Thus, for all the flashes in the overlap region in scans 62 blank shape code data are sent to shaper/blanker array 110. The substrate is then repositioned for the next scan, scan 63. The flashes in the upper overlap region of scan 63 are treated similarly to the flashes in the upper overlap regions of scans 61 and 62.

Flash 44,64 is the first flash in the overlap region of scan 64. Flash 44,64 has a pair of nonzero gray level value pixels in the lower half of the flash, thus flash 44,64 is not an special case overlap region first flash. Accordingly, flash 44,64 is treated according to the process

described in FIG. 2D. In stage 32, flash 44,64 and the pixels above the flash are checked for a pair of horizontal gray level value pixels. Flash 44,64 contains a horizontal pair of gray value pixels, thus the actual shape data for flash 44,64 are provided to shaper/blanker driver in stage 33 of FIG. 2D. In stage 36, the data in all the remaining flashes in the overlap region of scan 64 are
5 ignored.

Overlap region 80 forms the lower overlap region of stripe 82. The first flashes in the overlap region for scans 61-63 are each a special case overlap region first flash. Thus, each of these flashes is checked for a pair of horizontal zero gray level value pixels in the lower half of the flash and nonzero pixels in the upper half of the flash. Since each of flashes 44,61, 44,62,
10 and 44,63 has a pair of horizontal zeros in the lower half of the flash and nonzero pixels in the upper half of the flash, each of these flashes is the first flash written in the lower overlap region of its respective scan. Thereafter, each flash in the lower overlap region and in the nonoverlapping region in each scan is treated according to the process described in FIG. 2C.

Flash 44,64 is the first flash in the lower overlap region of scan 64. Flash 44,64 does not
15 have a pair of horizontal zeroes in the lower half of the pixels and nonzero pixels in the upper half of the pixel, thus flash 44,64 is treated according to the process described in FIG. 2B. Since flash 44,64 has a pair of zero gray value pixels in the flash, the pattern data in flash 44,64 are not written to the mask, shown in stage 24, but all remaining flashes in the lower overlap region of scan 64 are written to the mask, shown in stage 26.

20 According to the embodiment described in FIGS. 2B-2D, data in the lower overlap region of a scan are ignored until a flash with two zero gray level value pixels in the flash or in the pixels above the flash is detected. After a flash with a pair of horizontal zero gray level value pixels in the flash or above the flash is detected, that flash is ignored but all the flashes remaining in the lower overlap region and all the flashes in the center, nonoverlapping region of the scan
25 are written to the mask. The flashes are written in the upper overlap region of the scan until a

flash with a pair of horizontal zero gray level value pixels in the flash or in the pixels above the flash is detected. After such a flash is detected, that flash is written, but all the flashes in the upper overlap region above that flash are ignored and no data is written. Thus, each flash is written only once. In an overlap region, a boundary line of zero gray level value pixels detected in stage 22 of FIG. 2B and stage 32 of FIG. 2D determines which flashes are written in the upper overlap region of a lower scan or the lower overlap region of an upper scan. Dashed line 83 of FIG. 3 represents the boundary between features written in upper stripe 82 and features written in lower stripe 81, according to FIGS. 2B-2D. Thus, all features in the overlap region above line 83 are ignored in lower stripe 81. Blank shape code data are sent to shaper/blanker driver 110 for each flash above line 83 in lower stripe 81. Similarly, all features below line 83 are ignored in upper stripe 82. Blank shape code data are sent to shaper/blanker driver 110 for each flash below line 83 in upper stripe 82.

In the embodiment described above, features in the overlap region of the stripes are ignored in one stripe and written in the other stripe. Thus, such features can be written to the substrate more accurately than if the feature were split between two stripes. In addition, features are "moved" into the upper or lower stripe by flash converter 108. Flash converter 108 receives gray level data in the overlap region, then converts the gray level values to shape data or ignores the gray level values, based on the gray level values. Flash converter 108 can therefore move features to the upper or lower stripe while scanning. Therefore, no advance preparation of the data is required to sort the data into the upper or lower stripe.

Further, in order to convert a flash's pixels' gray level values to shape data, flash converter 108 reads not only the gray level values of the pixel, but also the gray level values of the pixels surrounding the flash. Thus, since the embodiment described above does not require data to be deleted from scans, it permits accurate conversion of the gray level values to shape code data. Also, a pattern is typically written on a substrate by scanning more than once. For

example a pattern may be scanned four times, with the boundaries between stripes in a different place for each scan. When the pattern is scanned four times, in each scan only a quarter of the energy necessary to expose the pattern on the substrate is used. Such a technique is time-consuming, but results in improved pattern resolution over a pattern that is scanned only once, because any errors associated with the edges of the stripes are averaged over multiple scans. The embodiment described above minimizes such stripe-edge associated errors and thus allows a pattern of acceptable resolution to be written in fewer scans or in a single scan.

Various modifications and adaptations of the embodiments and implementations described herein are encompassed by the attached claims.

CLAIMS

We claim:

1. In a raster scan lithography system, a method of preparing a mask comprising a plurality of features, the mask being represented by a pattern, the pattern comprising a plurality of overlapping horizontal stripes, the stripes further comprising a plurality of vertical scans, the vertical scans further comprising a plurality of flashes in a lower overlap region and a center region, each flash representing a portion of the pattern, the flashes comprising at least one pixel, each pixel assigned a gray level value describing a portion of the pixel covered by a feature, the method comprising:
 - receiving a first flash in the lower overlap region of a first scan, wherein at least one of a pixel in the first flash and a pixel above the first flash is assigned a gray level value indicating no portion of the pixel is covered by a feature;
writing on the mask a flash comprising no portion of a feature in a region of the mask represented by the first flash.
2. The method of Claim 1 further comprising:
prior to said receiving a first flash, receiving a second flash in the lower overlap region, wherein a pixel in the second flash is assigned a gray value indicating a portion of the pixel is covered by a feature; and
writing on the mask a flash comprising no portion of a feature in a region of the mask represented by the second flash.
3. The method of Claim 1 further comprising:
after said receiving a first flash, receiving a second flash; and
writing on the mask a portion of the pattern represented by the second flash.

4. The method of Claim 1 wherein the vertical scans further comprise a plurality of flashes in an upper overlap region, the method further comprising:
- receiving a second flash in the upper overlap region, wherein at least one of a pixel in a
- 5 the second flash and a pixel above the second flash is assigned a gray value indicating no portion of the pixel is covered by a feature; and
- writing on the mask a portion of the pattern represented by the second flash.
5. The method of Claim 4 further comprising:
- 10 prior to said receiving a second flash in the upper overlap region, receiving a third flash in the upper overlap region, wherein a pixel in a the third flash is assigned a gray value indicating a portion of the pixel is covered by a feature; and
- writing on the mask a portion of the pattern represented by the second flash.
- 15 6. The method of Claim 4 further comprising:
- after said receiving a second flash in the upper overlap region, receiving a third flash in the upper overlap region; and
- writing on the mask a flash comprising no portion of a feature in the region of the mask represented by the third flash.

20

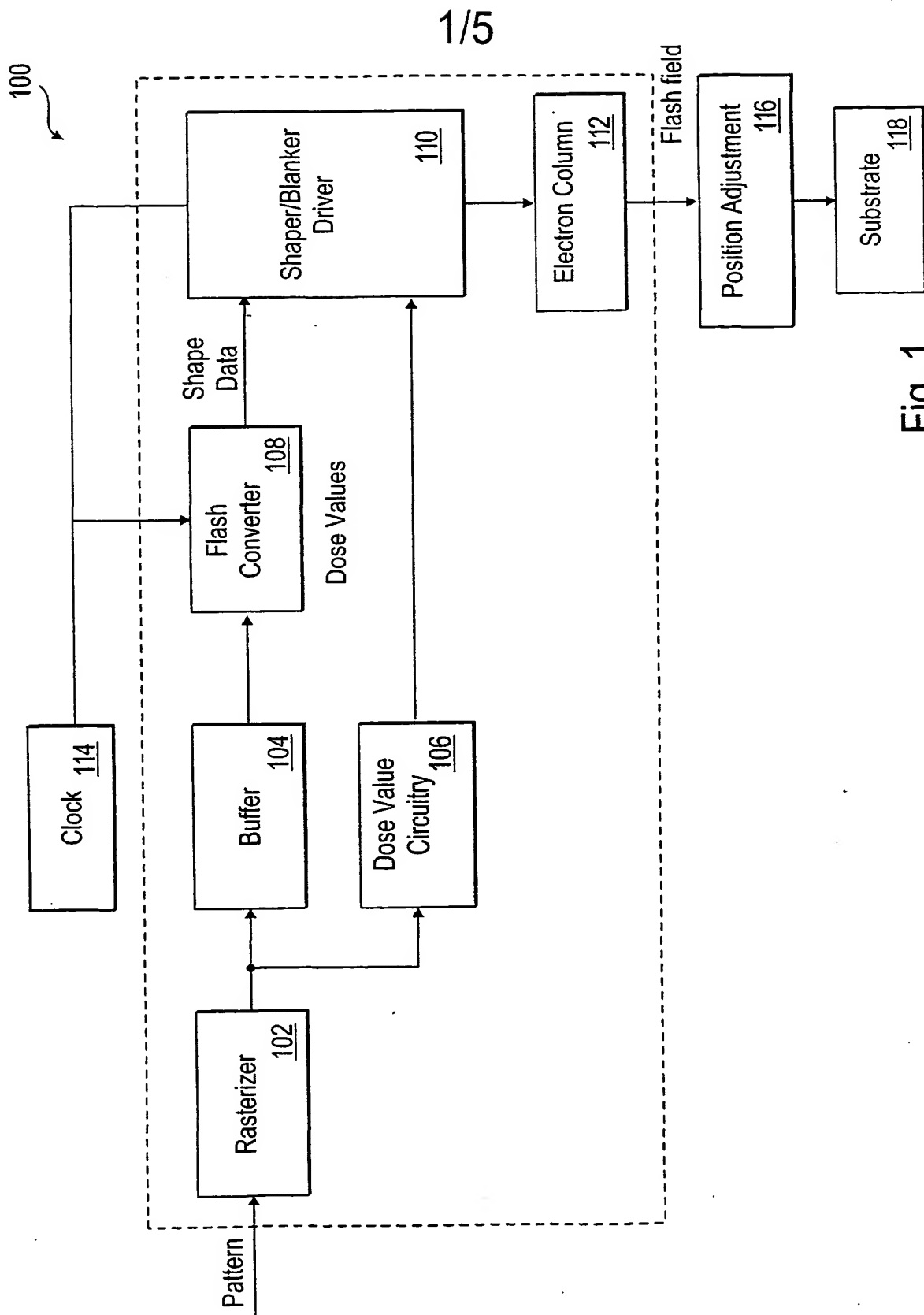


Fig. 1

2/5

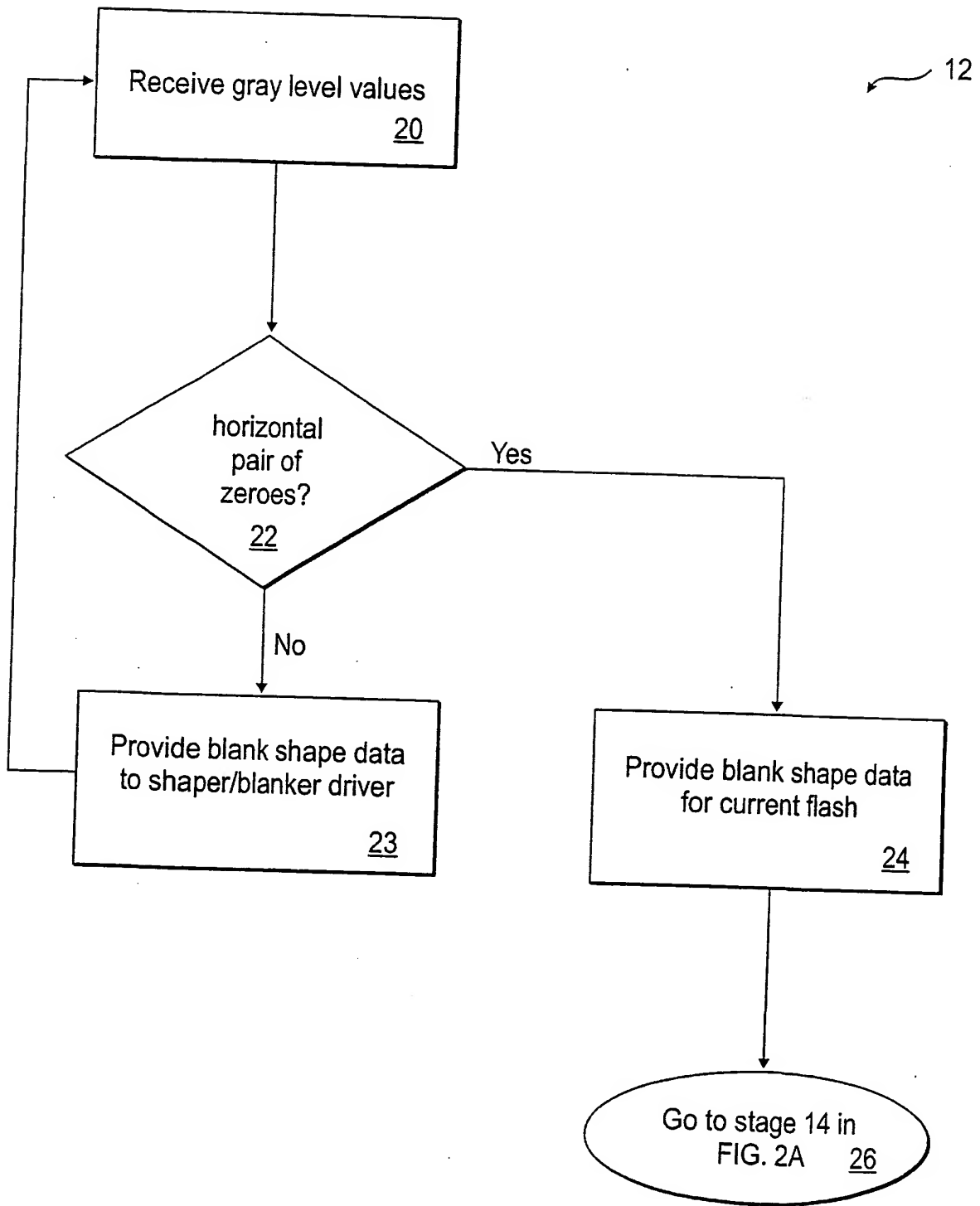
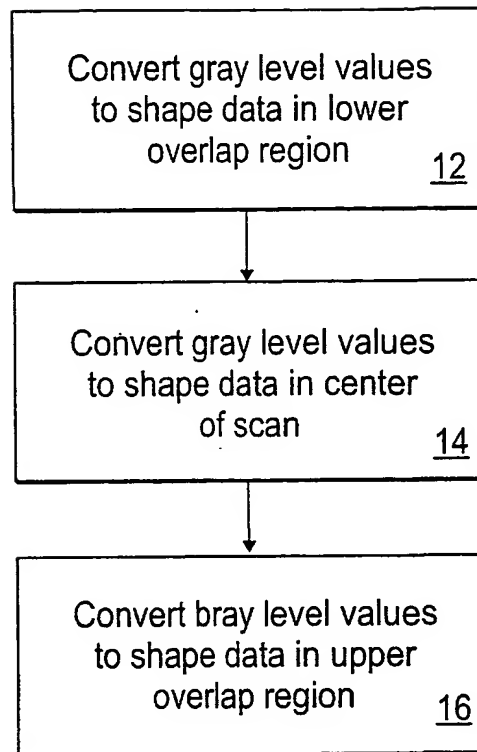


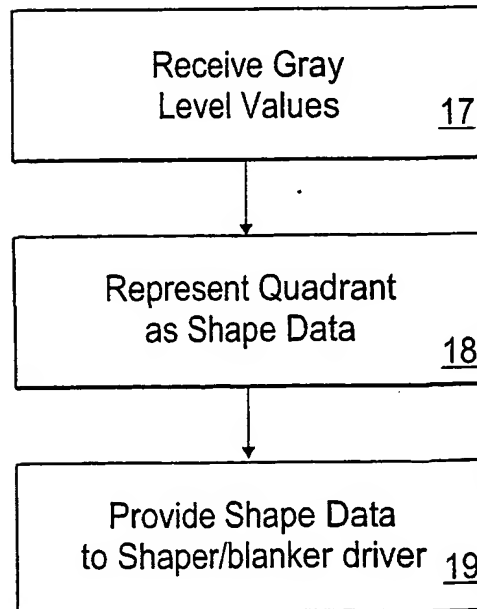
Fig. 2B

3/5



10

Fig. 2A



14

Fig. 2C

4/5

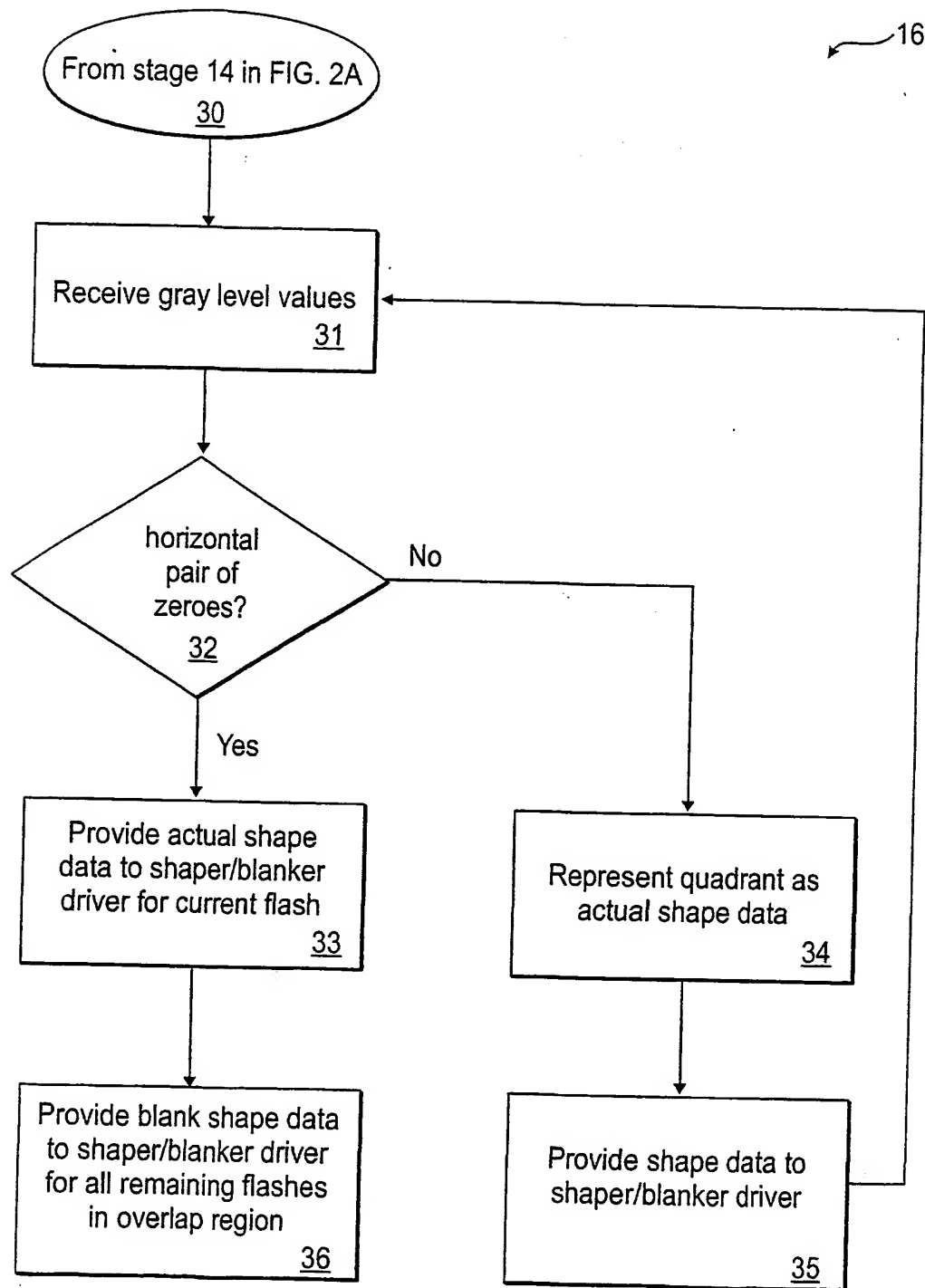


Fig. 2D

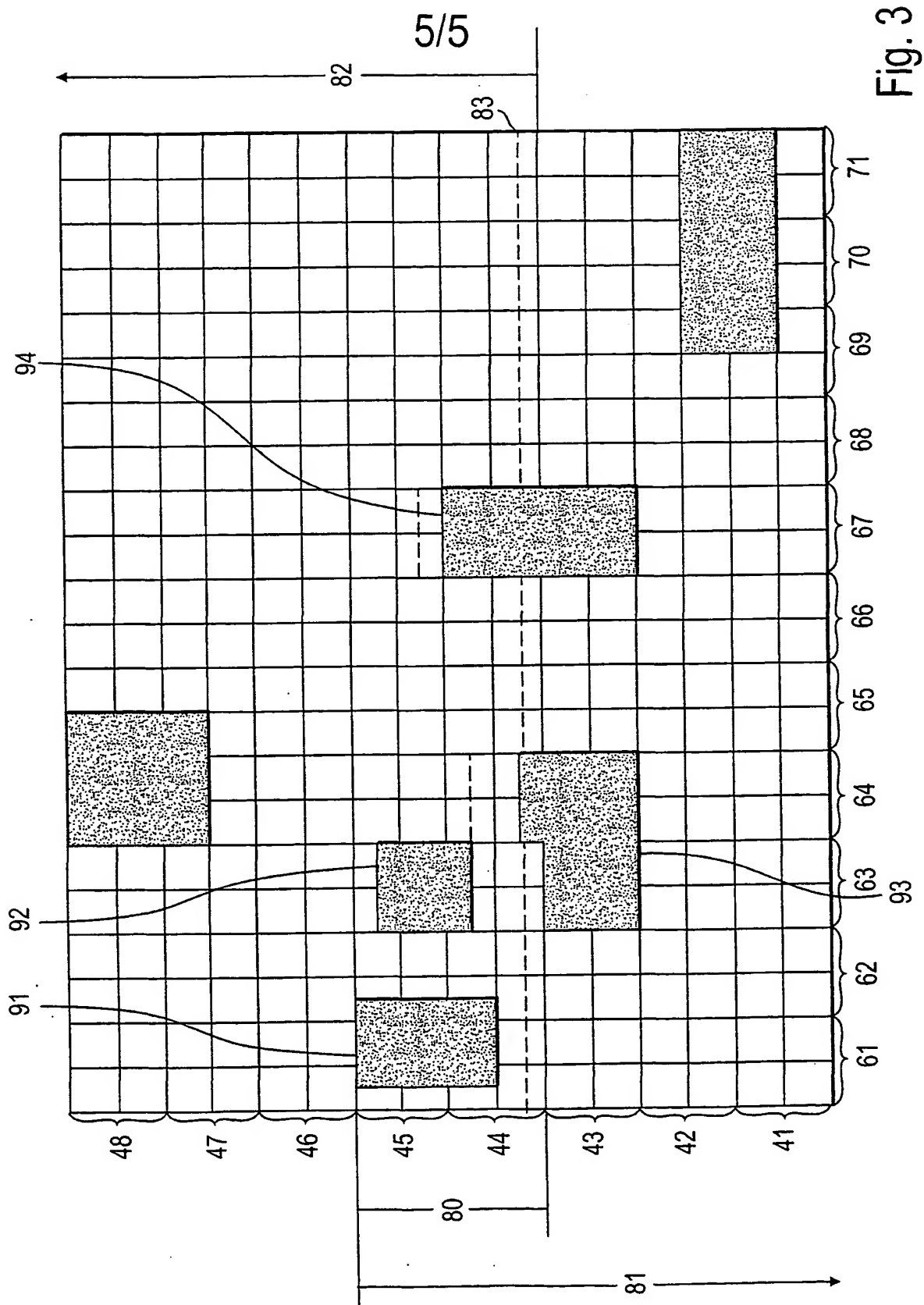


Fig. 3

SUBSTITUTE SHEET (RULE 26)

THIS PAGE BLANK (USPTO)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 February 2002 (21.02.2002)

PCT

(10) International Publication Number
WO 02/14952 A3

(51) International Patent Classification⁷: **H01J 37/302**,
37/317, G03F 7/20

(21) International Application Number: PCT/US01/25496

(22) International Filing Date: 14 August 2001 (14.08.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/639,381 14 August 2000 (14.08.2000) US

(71) Applicant: **APPLIED MATERIALS, INC.** [US/US]:
P.O. Box 450A, Santa Clara, CA 95052 (US).

(72) Inventors: **RISHTON, Stephen, A.**; 2511 Bishop Avenue, Fremont, CA 94536 (US). **LOZES, Richard, L.**:
P.O. Box 5340, Pleasanton, CA 94566-1340 (US).

(74) Agents: **BERNADICOU, Michael, A.** et al.: Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AT (utility model), AU, AZ, BA, BB, BG, BR, BY, BZ, CA,

CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(88) Date of publication of the international search report:
16 May 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 02/14952 A3

(54) Title: SCAN BUTTING ERROR REDUCTION IN A RASTER SCAN PATTERN GENERATION SYSTEM

(57) Abstract: A method and apparatus are disclosed for reducing scan butting error in a raster scan pattern generation system. A pattern to be written on a mask is first pixelized and each pixel is assigned a gray level value describing how much of the pixel is occupied by a feature to be written on the mask. The ends of each scan are overlapped with the neighboring scans. In each scan, no pattern data is written to the mask in the lower overlap region of the scan until a blank pixel or a pair of blank pixels is detected, i.e. a pixel or pair of pixels that do not contain any part of a feature to be written on the mask. After such a pixel or pair of pixels is detected, the pattern data for each flash is written to the mask until another blank pixel or pair of blank pixels is detected in the upper overlap region of the scan. No pattern data is written to the mask for the flashes in the scan that are scanned after the pair of blank pixels.

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01J37/302 H01J37/317 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC.

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 G03F H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 766 802 A (SKINNER JOHN G) 16 June 1998 (1998-06-16) cited in the application column 3, line 39 - line 67 column 5, line 42 - column 7, line 50 figure 4	1
X	WO 98 33096 A (MICRONIC LASER SYSTEMS AB ;THUREN ANDERS (SE); SANDSTROEM TORBJOER) 30 July 1998 (1998-07-30) page 14, line 31 -page 16, line 26 figures 4-6	1

☐ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents:

A document defining the general state of the art which is not considered to be of particular relevance

E earlier document but published on or after the international filing date

L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

1 March 2002

Date of mailing of the international search report

12/03/2002

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Aguilar, M.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 01/25496

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
US 5766802	A	16-06-1998	WO	9735235 A1	25-09-1997
WO 9833096	A	30-07-1998	WO	9833096 A1	30-07-1998
			AU	2048097 A	18-08-1998
			EP	0956516 A1	17-11-1999

THIS PAGE BLANK (USPTO)